IN THE CLAIMS

Please cancel Claim 15 and Amend the remaining claims in accordance with the following markup:

13. (Currently Amended) A method for manufacturing an integrated circuit substrate, comprising:

embossing a top side of the substrate with a tool having features defining a reverse image of channels for addition of circuit material; ~~and~~

adding circuit material within channels formed by the embossing; [[.]]

embossing a bottom side of the substrate with a second tool having features defining a reverse image of bottom channels for addition of bottom circuit material; and

second adding circuit material within the bottom channels formed by the second embossing.

14. (Original) An integrated circuit manufactured by the method of Claim 13.

15. (Canceled)

16. (Currently Amended) The method of Claim 1~~3~~5, wherein the substrate comprises a top insulating layer and bottom insulating layer bonded on opposite sides of a metal layer, wherein the method further comprises perforating the metal layer prior to bonding the insulating layers to the metal layer.

17. (Original) The method of Claim 16, wherein the perforating is performed by etching the metal layer.

18. (Currently Amended) The method of Claim 1~~3~~5, wherein the second tool has features for creating voids through the substrate from the channels to the bottom channels, and wherein the method further comprises depositing circuit material within the voids for electrically connecting circuit material within the channels to circuit material within the bottom channels.

19. (Currently Amended) The method of Claim 1~~3~~5, further comprising mounting a flip-chip die having electrical contacts on [[a]] the bottom side by inserting the electrical contacts within the channels formed by the embossing.

20. (Currently Amended) The method of Claim 1~~3~~5, wherein the embossing forms a void through the substrate for insertion of a mounting post, and further comprising:

mounting a die having a retaining post on a top side of the substrate, by inserting the retaining post through the void; and

soldering the retaining post to circuit material on [[a]] the bottom ~~the~~ side of the substrate.

21. (Original) The method of Claim 13, wherein the adding is performed by electroplating copper on the top side of the substrate and wherein the method further comprises:

depositing a resist material on top of areas of the circuit material; and

etching the electroplated copper to form an electrical circuit within the areas.

22. (Original) The method of Claim 13, wherein the adding is performed by electroplating copper on the top side of the substrate, and wherein the method further comprises:

plating areas of the electroplated copper with a metal resistant to the etching within areas of the circuit material; and

etching the electroplated copper, wherein the electroplated copper is retained under the areas.

Claims 23-25 (canceled)

26. (Previously Presented) The method of Claim 13, further comprising providing a homogeneous single sheet of dielectric material, and wherein the embossing embosses the top side of the dielectric material to form the channels.

27. (Previously Presented) The method of Claim 26, wherein the embossing embosses channels having sides extending to a plane defining a top surface of the dielectric sheet and a bottom beneath the plane.

28. (Currently Amended) The method of Claim 27, wherein the embossing embosses channels having a bottom of the channels [[is]] located at a second plane substantially above the bottom surface of the dielectric sheet.

29. (Previously Presented) The method of Claim 28, further comprising bonding the dielectric sheet to a metal layer prior to the embosssing.

30. (Previously Presented) The method of Claim 13, wherein the embossing embosses channels having sides extending to a plane defining a top surface of the substrate and a bottom beneath the plane.

31. (Currently Amended) The method of Claim 30, wherein the embossing embosses channels having a bottom of the channels [[is]] located at a second plane substantially above the bottom surface of the substrate.

32. (Previously Presented) The method of Claim 13, wherein the adding comprises applying a gold foil within the channels.

33. (Previously Presented) The method of Claim 13, further comprising electrically connecting an integrated circuit die to the circuit material within the channels.

34. (Previously Presented) The method of Claim 33, wherein the electrically connecting is performed by adding bonding wires between the circuit material and electrical terminals of the die.

35. (Previously Presented) The method of Claim 33, wherein the electrically connecting is performed by directly bonding electrical terminals of the die to the circuit material.

36. (Previously Presented) The method of Claim 13, further comprising prior to the embossing, stamping a metal foil to form the reverse image of the channels.

37. (Previously Presented) The method of Claim 36, further comprising mounting the stamped metal foil to a tooling plate.

38. (Previously Presented) A method for manufacturing an integrated circuit, comprising:

first embossing a top side of a top outer dielectric layer of a substrate with a tool having features defining a reverse image of top channels for addition of circuit material, the top channels having sides extending to a plane defining a top surface of the substrate and a bottom beneath the plane, wherein the bottom of the top channels is located at a second plane substantially above the bottom surface of the top outer dielectric layer;

adding circuit material within the channels formed by the embossing; and

electrically connecting an integrated circuit die to the circuit material within the channels.

39. (Previously Presented) The method of Claim 38, further comprising second embossing a bottom side of a bottom outer dielectric layer of the substrate with a tool having features defining a reverse image of bottom channels for addition of circuit material, the bottom channels having sides extending to

a third plane defining a bottom surface of the substrate and a bottom beneath the third plane, wherein the top of the bottom channels is located at a second plane substantially below the top surface of the bottom outer dielectric layer; and

adding bottom circuit material within bottom channels.

40. (Previously Presented) The method of Claim 39, further comprising providing a homogeneous single sheet of dielectric material, and wherein the first embossing embosses the top side of the dielectric sheet to form the top channels and the second embossing embosses the bottom side of the dielectric sheet to form the bottom channels.